L Number	Hits	Search Text	DB	Time stamp
1	5047	(vhdl or verilog or hdl or (hardware with	USPAT	2003/11/21 18:54
		(definition or design) with language\$1))		
2	3878	((vhdl or verilog or hdl or (hardware with	USPAT	2003/11/21 18:56
		(definition or design) with language\$1)))		
	2617	and @ad<19990902		
6	3617	(((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:02
		with (definition or design) with language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		1
		function\$1 or procedure\$1)		
7	3493	((((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:03
		with (definition or design) with		2000, 11, 21 13.00
		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		İ
		function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
1		pre\$1determin\$3)		
8	3364	(((((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:03
		with (definition or design) with language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3		
]		or assign\$3 or set\$4 or defin\$3 or	İ	
		pre\$1determin\$3)) and (initial or starting		
		or first or beginning)]
9	2660	((((((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:04
[with (definition or design) with		
l i		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
		pre\$1determin\$3)) and (initial or starting		·
		or first or beginning)) and (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1		1
		or reg\$2 or register\$1)		
10	2606	((((((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:06
		with (definition or design) with	001111	2003/11/21 13:00
		language\$1))) and @ad<19990902) and		
1		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
		pre\$1determin\$3)) and (initial or starting		
		or first or beginning)) and (node\$1 or		
		signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1		
		or reg32 or register31)) and (condition\$1 or value\$1 or voltage\$1 or state\$1)		
11	1211	(((((((vhdl or verilog or hdl or	USPAT	2003/11/21 19:06
		(hardware with (definition or design) with	OSTAT	2003/11/21 19.00
		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
1		<pre>function\$1 or procedure\$1)) and (initial\$3</pre>		
		or assign\$3 or set\$4 or defin\$3 or		
		<pre>pre\$1determin\$3)) and (initial or starting</pre>		
		or first or beginning)) and (node\$1 or		
		signal\$1 or variable\$1 or wire\$1 or port\$1		
		or reg\$2 or register\$1)) and (condition\$1		
		or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or		
		beginning) same (node\$1 or signal\$1 or		
		variable\$1 or wire\$1 or port\$1 or reg\$2 or		
		register\$1) same (condition\$1 or value\$1		
		or voltage\$1 or state\$1))		
			L.,.	<u> </u>

726 (((((((((vhdl or verilog or hdl or (hardware with (definition or design) with language\$1))) and @ad<19990902) and (module\$1 or sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1)) and (initial\$3 or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3)) and (initial or starting or first or beginning)) and (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1 or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or beginning) with (node\$1 or signal\$1 or	/21 19:08
<pre>(module\$1 or sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1)) and (initial\$3 or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3)) and (initial or starting or first or beginning)) and (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1 or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or</pre>	
pre\$ldetermin\$3)) and (initial or starting or first or beginning)) and (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1 or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or	
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register\$1) with (condition\$1 or value\$1 or voltage\$1 or state\$1)) 13 510 ((((((((((vhdl or verilog or hdl or USPAT 2003/11	/21 19:09
(hardware with (definition or design) with language\$1))) and @ad<19990902) and	21 19.09
<pre>(module\$1 or sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1)) and (initial\$3</pre>	
or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3)) and (initial or starting or first or beginning)) and (node\$1 or	
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or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or	
beginning) with (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1) with (condition\$1 or value\$1	
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or state\$1))) 14	/21 19:10
(hardware with (definition or design) with language\$1))) and @ad<19990902) and (module\$1 or sub\$1routine\$1 or header\$1 or	
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or voltage\$1 or state\$1))) and ((initial\$3 or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3) same ((initial or	
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or state\$1)))) and ((module\$1 or sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1) same ((initial\$3 or	
assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3) same ((initial or	
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with (condition\$1 or value\$1 or voltage\$1 or state\$1)))	

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15	16	(((((((((vhdl or verilog or hdl or	USPAT	2003/11/21 19:12
		(hardware with (definition or design) with		
		language\$1))) and @ad<19990902) and		İ
ŀ		(module\$1 or sub\$1routine\$1 or header\$1 or		
	1	function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
		pre\$1determin\$3)) and (initial or starting		
		or first or beginning)) and (node\$1 or		
i		signal\$1 or variable\$1 or wire\$1 or port\$1		
		or reg\$2 or register\$1)) and (condition\$1		
		or value\$1 or voltage\$1 or state\$1)) and		
		((initial or starting or first or		
		beginning) with (node\$1 or signal\$1 or		İ
		variable\$1 or wire\$1 or port\$1 or reg\$2 or		i
	ļ	register\$1) with (condition\$1 or value\$1		
		or voltage\$1 or state\$1))) and ((initial\$3		
1		or assign\$3 or set\$4 or defin\$3 or		
1		pre\$1determin\$3) same ((initial or	ĺ	
		starting or first or beginning) with		
	l	(node\$1 or signal\$1 or variable\$1 or		
		wire\$1 or port\$1 or reg\$2 or register\$1)		
		with (condition\$1 or value\$1 or voltage\$1		
		or state\$1)))) and ((module\$1 or		
		sub\$1routine\$1 or header\$1 or function\$1		
		or procedure\$1) same ((initial\$3 or		
		assign\$3 or set\$4 or defin\$3 or		
		pre\$1determin\$3) same ((initial or		
		starting or first or beginning) with		
		(node\$1 or signal\$1 or variable\$1 or		
İ		wire\$1 or port\$1 or reg\$2 or register\$1)		
		with (condition\$1 or value\$1 or voltage\$1		
		or state\$1))))) and ((releas\$3 or free\$3)		
		same ((initial or starting or first or		
		beginning) with (node\$1 or signal\$1 or		
		variable\$1 or wire\$1 or port\$1 or req\$2 or		
1		register\$1) with (condition\$1 or value\$1		
		or voltage\$1 or state\$1)))		
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